CLAIMS:

1. A digital information system comprising a digital signal source and a memory card with playback function connected with the digital signal source to receive and store a specified digital signal in a memory and to reproduce the digital signal stored independently.

2. A digital information system according to Claim 1, wherein a digital signal is received/delivered between the digital signal source and the memory card with playback function at a rate at least higher than the signal processed.

3. A digital information system according to Claim 1, comprising a digital signal source and a memory card with playback function connected to the digital signal source for receiving/delivery of the digital signal, the memory card having a memory receiving and storing a specified digital signal and reproducing a digital signal stored independently, wherein said digital signal source includes a digital signal supply and a terminal device for storing a digital signal received from the digital signal supply through selected one of a communication channel and an appropriate storage medium as required, said terminal device being connected through a connector to the memory card with playback function for receiving/delivery of a specified digital signal.

4. A digital information system according to Claim 3, wherein the storage capacity of the terminal device is equal to or more than that of the memory on the memory card with playback function.

5. A digital information system according to Claim 3, wherein the terminal device includes a magnetic disk memory having a comparatively large storage capacity as a backup memory, and selected one of a digital signal received/delivered in large amount with the memory card with playback function and a digital signal updated with time is stored in a buffer memory including a semiconductor memory accessible at high speed.

6. A digital information system according to Claim 3, wherein the terminal device has a function as a microcomputer for managing the magnetic disk memory and the buffer memory and exchanging a digital signal with a digital signal supply through a communication channel, said terminal device further managing the storage area for a memory in the memory card with playback function connected thereto.

7. A digital information system according to Claim 4, wherein the terminal device has a function as a microcomputer for managing the magnetic disk memory and the buffer memory and exchanging a digital signal with a digital signal supply through a communication channel, said terminal device further managing the storage area

for a memory in the memory card with playback function connected thereto.

8. A digital information system according to Claim 5, wherein the terminal device has a function as a microcomputer for managing the magnetic disk memory and the buffer memory and exchanging a digital signal with a digital signal supply through a communication channel, said terminal device further managing the storage area for a memory in the memory card with playback function connected thereto.

9. A digital information system according to Claim 3, wherein said terminal device has the function of reproducing and outputting a part of a designated digital signal for a predetermined length of time.

10. In a digital information system comprising a digital signal source and a memory card connected with the digital signal source in receiving/delivery of a digital signal and having a memory for storing a specified digital signal, said memory card reproducing a digital signal stored independently, said memory card with playback function having a secondary battery built therein, said secondary battery being charged by a power supply on the terminal device side when connected with the terminal device.

11. A memory card with playback function according to Claim 10, comprising a playback circuit for outputting a digital audio signal read out of a memory by being converted into an analog audio signal.

12. A memory card with playback function according to Claim 11, which is selected one of separable and removable as a thin card-like storage medium.

13. A memory card with playback function according to Claim 11, comprising an ID code (1308), wherein the playback conditions are automatically designated in accordance with the contents of the ID code.

14. A memory card with playback function according to Claim 13, wherein the playback conditions include at least one of the stereo/monaural playback, a resolution of 8 and 16 bits and a sampling frequency.

15. In a digital information system comprising a digital signal source and a memory card with playback function connected with the digital signal source in receiving/delivery of a digital signal, said memory card having a memory for receiving and storing a specified digital signal and reproducing a digital signal stored independently, said memory storing and controlling the digital signal, a connectors for receiving/delivery of a signal from an external source and an operating section for controlling the playback.

16. A memory card with playback function according to Claim 15, wherein said connector for receiving/delivery of a digital signal is conforming to selected one of JEIDA standard and equivalent standard.

17. In a digital information system comprising a digital signal source and a memory card with playback function connected to the digital signal source in

receiving/delivery of the digital signal, said memory card having a memory for receiving and storing a specified digital signal, said memory card reproducing a digital signal stored independently, wherein said memory has a security function of performing selected one of the operations of inverting at least one-bit digital signal of the input and/or output section of the memory in accordance with selected one of a password and a password coincidence detection signal and replacing the digital signal with another bit thereby to prevent the user from reproducing a correct digital signal.

18. A memory according to Claim 17, comprising a security function wherein at least a one-bit digital signal of the address input section of the memory is subjected to selected one of being inverted and replaced with another bit in accordance with selected one of a password and a password coincidence detection signal thereby preventing the user from reproducing a correct digital signal.

19. A memory according to Claim 17, comprising a security function for performing selected one of the operations of nullifying and replacing with another bit at least one-bit digital signal of the output section of the memory in accordance with selected one of a password and a password coincidence detection signal thereby to prevent a correct digital signal from being read out from the memory card with playback function.

20. A memory according to Claim 17, comprising a security function for performing selected one of the operations of nullifying and replacing with another bit at least one bit of digital signal at the address input section of the memory in accordance with selected one of a password and a password coincidence signal thereby to prevent a correct digital signal from being read out from the memory card with playback function.

21. A memory according to Claim 17, which is divided into given storage capacities thereby to store a plurality of different types of information, wherein the user can select a given type of information from the stored information at the time of playback.

22. A memory according to Claim 17, comprising selected one of a storage area and a contents memory for storing contents information having storage addresses corresponding to a plurality of digital signals and selected one of a data area and a data memory accessible from the storage addresses.

23. A memory card with playback function according to Claim 15, wherein said operating section designates a plurality of types of operating mode by selected one of on time and the number of turnings on of a single key switch.

24. A digital information system comprising a digital signal source and a memory card with playback function connected with the digital signal source for receiving a specified digital signal, storing the same

digital signal in a memory and reproducing the stored digital signal independently,

said system further comprising means for performing selected one of the operations of compressing and extending the information amount in comparison with the original information amount of the digital signal and noise-neglecting means for removing noises.

25. A digital information system according to Claim 24, wherein said noise-neglecting means includes means for detecting a voice interval of a digitized audio signal and means for forcibly replacing the digital signal inputted to a digital-to-analog converter with a signal corresponding to an AC-like 0 level.

26. A digital information system according to Claim 24, further comprising comparator means for comparing a digital signal with predetermined positive and negative levels considered voiceless as a voice interval, wherein a predetermined period within a predetermined level is considered voiceless on the basis of the result of comparison.

27. A digital information system according to Claim 24, wherein said extension means detects a voice interval of a digitized audio signal, and said means for enlarging the voice interval performs the slow playback.

28. A digital information system according to Claim 27, wherein said means for enlarging the voice interval substantially delays the address-updating

operation of a memory storing a digital signal as compared with the normal operation.

29. A digital information system according to Claim 24, wherein said compression means detects a voice interval of a digitized audio signal and shortens the voice interval for fast playback.

30. A digital information system according to Claim 29, wherein said means for shortening the voice interval increases the speed of the address-updating operation of a memory storing a digital signal as compared with the normal operation.

31. A digital information system according to Claim 24, wherein said compression means includes

means for determining the difference between the immediately preceding sampling data of the digital signal and an input data,

means for outputting the maximum value of a compressed data when the difference is larger than the maximum value of a compressed code, and

means for outputting the result of subtraction on the basis of the compressed data when the difference is smaller than the maximum value of the compressed code.

32. A digital information system according to Claim 24, wherein said extension means extends the data of the digital signal into the original data by adding the immediately preceding sampling data thereto.

33. A digital signal processor comprising:

means for compressing a data by replacing a voice interval of a digital signal with a voice interval code data and a voice interval time data;

means for stopping the address-updating operation of a memory over a time length corresponding to the voice interval time data and outputting a signal corresponding to an AC-like 0 level when a voice interval code data is detected in normal operation;

means for stopping the address-updating operation of a memory over a time length enlarged against the voice interval time data and outputting a signal corresponding to an AC-like 0 level when a voice interval code data is detected in slow playback mode; and

means for ignoring the voice interval code data and the voice interval time data substantially and outputting a digital signal in fast playback mode.

34. A digital signal processor according to Claim 33, wherein said voice interval code data includes a combination of at least two successive digital signals corresponding to a substantially positive maximum value and a substantially negative maximum value.

35. A digital signal processor according to Claim 33, wherein a maximum voice interval is set, said processor including the function of limiting the voice interval enlarged with the slow playback not to exceed the maximum voice interval.

36. A signal converter comprising:

a memory for receiving a digital input signal;

a counter for performing the counting operation corresponding to the maximum value of a digital input signal in response to a reference time pulse;

a comparator for comparing an output signal of the memory with an output signal of the counter;

a repeat counter for counting the repetitions of the counting operation of the counter; and

a controller for instructing the memory to receive an input digital signal in response to a strobe signal, causing the counter to start the counting operation, and sending out a conversion-over signal in response to an output signal from the repeat counter,

wherein a pulse-width modulated signal corresponding to a digital input signal is produced from the output of the comparator.

37. A signal converter comprising:

a down counter for counting reference time pulses in response to a digital input signal supplied at a predetermined period corresponding to the maximum value of the digital signal, and

a digital circuit for forming a pulse corresponding to the operation time of the down counter,

thereby producing a pulse width modulated signal corresponding to the digital input signal.

38. A signal converter according to Claim 37, wherein the predetermined period corresponding to the

maximum value of the digital signal is formed by an up counter for performing the counting operation corresponding to the digital input signal in response to the reference time pulse.

39. A signal converter according to Claim 36, wherein said pulse width modulated signal is inputted to and converted into an analog signal by a low-pass filter including a resistor and a capacitor.

40. In a digital audio signal playback circuit comprising a memory for storing a digital audio signal, means for reading the digital audio signal from the memory independently, a digital-to-analog converter for converting the digital audio signal to an analog audio signal, a low-pass filter, and an amplifier for amplifying a signal inputted thereto through the low-pass filter,

a one-chip integrated circuit comprising a digital-to-analog converter, a low-pass filter, an amplifier, a controller and an interface section except for the memory.

41. In said digital audio signal playback circuit, a one-chip integrated circuit according to Claim 40, further having the function of enlarging the memory control function outside the one-chip integrated circuit easily when the storage capacity exceeds a controllable level.

42. A one-chip integrated circuit according to Claim 40, wherein the interface section comprises:

a signal terminal for realizing the data transfer of the digital signal receiving/delivery system;

a signal terminal for controlling the storage capacity;

a signal terminal for outputting an analog audio signal;

a signal terminal for supporting the operation of the digital audio signal playback circuit;

a signal terminal for indicating the state of the digital audio signal playback circuit; and

a signal terminal for supplying power to the one-chip integrated circuit.

43. In said digital audio signal playback circuit, a digital audio playback circuit according to Claim 40, further comprising the step of skipping the address of a defective part of the memory by self-diagnosis conducted when information is written into the memory.

44. In said digital audio signal playback circuit, a digital audio playback circuit according to Claim 41, further comprising the step of skipping the address of a defective part of the memory by self-diagnosis conducted when information is written into the memory.

45. In said digital audio signal playback circuit, a digital audio playback circuit according to Claim 42, further comprising the step of skipping the address of a defective part of the memory by self-diagnosis conducted when information is written into the memory.